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V/F CONTROL OF INDUCTION MACHINE USING FPGA ALTERA

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Abstract - This paper presents an FPGA-based constant voltage-to-frequency (V/f) control system for three-phase induction motors using the Altera DE0-Nano development board. The V/f control technique maintains a constant voltage-to-frequency ratio to preserve optimal motor flux and torque characteristics across the operating range. The complete control algorithm was developed in Verilog HDL using Quartus Prime Lite, generating sinusoidal PWM signals with programmable dead-time insertion for inverter protection and featuring UART communication for real-time speed control with ramping capabilities. Simulation and experimental testing validated accurate V/f ratio maintenance, precise speed control, and stable motor operation across multiple speed references. The key achievement is demonstrating that low-cost FPGA platforms integrated with low-cost UART modules can deliver professional-grade motor control with real-time responsiveness and implementation flexibility, avoiding the limitations of platform-specific tools like Simulink. The system establishes FPGA technology as a viable, economical alternative to traditional DSP-based or high-range FPGA drives.

Index Terms - FPGA, Induction motor, Pulse width modulation, V/f control.

INTRODUCTION

Variable voltage variable frequency (V/f) control represents one of the most widely implemented methods for induction motor speed control in industrial applications due to its simplicity, reliability, and cost-effectiveness. This project demonstrates the design and implementation of a V/f control system for a three-phase induction motor using the Altera DE0-Nano FPGA development board. By maintaining a constant voltage-to-frequency ratio, the control strategy ensures that the motor's magnetic flux remains constant across the operating speed range, thereby preserving optimal torque characteristics and preventing magnetic saturation or motor instability [1].

The implementation leverages the parallel processing capabilities and real-time performance of Field-Programmable Gate Arrays (FPGAs), which offer significant advantages over traditional microcontroller-based solutions in terms of execution speed, deterministic timing, and flexibility. Unlike processors that execute software instruction sequences sequentially, the configuration of an FPGA defines a physical hardware circuit customized for a specific task, allowing for highly parallel and deterministic operation [2].

A primary motivation for this work was to prove that a capable induction motor controller could be built on a relatively low-cost and accessible platform like the Altera DE0-Nano FPGA. A key distinction of this project is the implementation of the core logic in Verilog HDL. This approach was chosen because Verilog HDL is compatible with virtually any FPGA, unlike higher-level tools such as MATLAB Simulink, which may not fully support specific chip families, such as the Cyclone IV FPGA used on the DE0-Nano, without expensive additional packages. Furthermore, the project addresses the gap in existing literature, which largely focuses on high-range Xilinx FPGAs [3], by successfully implementing V/f control on a compact Intel Altera platform. The complete control algorithm was developed in Verilog HDL using Quartus Prime Lite [4].

The paper is structured as follows: Section II outlines the theoretical background of V/f control and PWM. Section III details the system design and implementation logic.

Section IV presents the simulation and experimental results, and Section V concludes the paper.

THEORETICAL BACKGROUND

I. V/f Control and SPWM

V/f control, or scalar control, maintains a constant ratio between the stator voltage and the supply frequency to ensure the motor's magnetic flux remains stable during speed variation. The fundamental ratio is defined as:

$$\frac{V}{f} = k \quad (1)$$

where k is the constant Volts-per-Hertz ratio. To generate the variable voltage and frequency output, the system employs Sinusoidal Pulse Width Modulation (SPWM). This technique involves comparing a high-frequency triangular carrier wave with a low-frequency sinusoidal reference wave. The frequency of the sinusoidal reference sets the output frequency, while the amplitude controls the fundamental output voltage amplitude [5].

The synchronous speed of the induction motor is determined by:

$$\frac{120 \times f}{P} = N \quad (2)$$

where N is the synchronous speed in RPM, f is the supply frequency in Hz, and f is the number of poles. The SPWM implementation on the FPGA allows for simultaneous generation of three 120-degree phase-shifted PWM signals with deterministic timing, essential for driving the three-phase inverter efficiently.

II. Hardware Platform

The core controller is the Altera DE0-Nano board, featuring a Cyclone IV FPGA (EP4CE22F17C6N) [6]. This platform offers 22,320 Logic Elements (LEs) and 72 digital I/O pins, sufficient for the complete control system. A critical advantage of this board for motor control is the parallel processing capability, enabling the simultaneous handling of PWM generation, V/f calculations, and communication protocols.

For user interface, the FT232RL USB-to-UART serial converter module bridges the host computer and the FPGA. It translates USB signals into UART protocol, allowing real-time speed commands to be transmitted from the Arduino IDE serial interface to the FPGA control logic.

DESIGN AND IMPLEMENTATION

The design implements the V/F motor control as a set of concurrent hardware modules described in Verilog HDL [7]. The system architecture, depicted in Fig. 1, consists of a UART receiver, a ramp controller, a V/f calculator, a sine look-up table (LUT), and SPWM generation logic with dead-time insertion.

I. System Architecture

The overall system structure is designed to manage the flow of data from user input to the inverter output [8]. Figure 2 illustrates the block diagram of the implemented control logic. Utility power passes through protection and an autotransformer into the inverter, which supplies the induction motor. On the control side, the user enters the desired speed via the Arduino IDE serial interface; the FPGA receives this command over UART and smoothly adjusts both the output frequency and the amplitude of the three-phase reference waveforms.

II. Communication and Ramping

The system receives speed commands in RPM via the UART module. The received ASCII characters are converted to integer values representing the desired speed. The FPGA then calculates a target V/f scaling factor, denoted as **K_NUM_target**. For a motor rated at 3000 RPM, the ratio is calculated as:

$$\mathbf{K_{NUM_{target}}} = \frac{speed\_rpm \times 100}{3000} \quad (3)$$

To prevent abrupt changes in voltage and frequency that could damage the motor, a ramping algorithm is

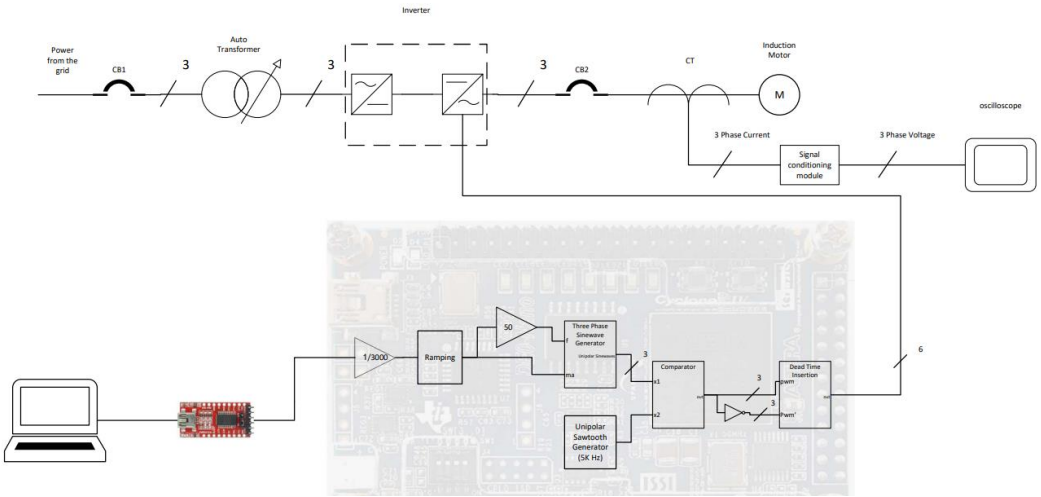

Figure 1. The design diagram showing power and control paths.

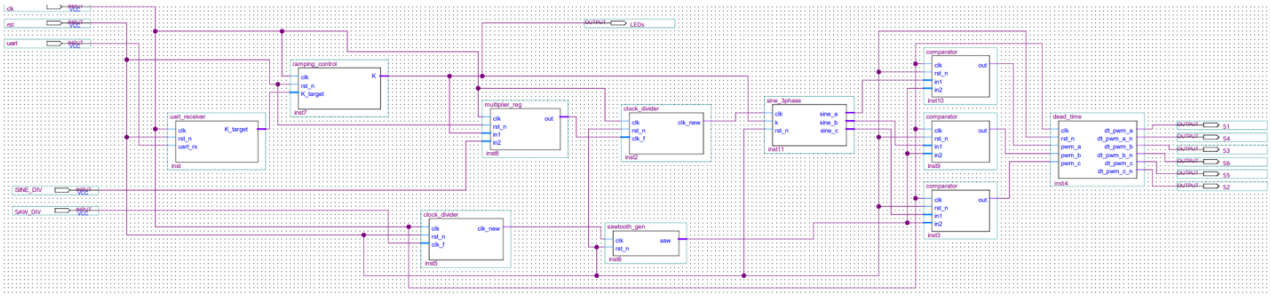

Figure 2. System block diagram of the V/f control implementation.

implemented. The algorithm increments or decrements the actual scaling factor **K_NUM** toward the target value in unit steps, with a programmable delay (e.g., 20 ms per unit step). This ensures smooth acceleration and deceleration.

III. Sine Generation and V/f Logic

A 512-entry sine LUT stores discrete samples of a sine wave cycle. Three-phase sine waves are generated by reading values from the LUT with phase offsets of 0, 120, and 240 degrees. The amplitude of these reference sine waves is scaled dynamically based on the **K_NUM** value to maintain the constant V/F ratio.

A frequency calculation block determines the sampling rate for the LUT based on the current **K_NUM**. A sawtooth carrier wave is generated using a simple counter. The SPWM signals are produced by comparing the scaled sine wave values with the sawtooth carrier.

IV. Dead-Time Insertion

Dead time is a critical safety feature implemented to prevent shoot-through faults in the voltage source inverter. The logic inserts a programmable delay (set to 2 µS) between the switching of complementary signals (e.g., between the high-side and low-side switches of the same phase). This is achieved by delaying the rising edges of the PWM pulses while maintaining the dead-time constraints defined by IEC 61800-5-1.

RESULTS AND DISCUSSION

The system was validated through simulation in Simulink and Questa Simulation Software, followed by experimental testing on a laboratory three-phase induction motor.

I. Simulation Results

Before hardware implementation, the expected system performance was validated through simulation in MATLAB/Simulink. Figure 3 shows the Simulink model used to generate balanced three-phase sinusoidal reference signals for sinusoidal pulse-width modulation (SPWM). These references are compared with a high-frequency carrier producing the inverter switching signals, as illustrated in Figure 4. The resulting SPWM-controlled inverter supplies balanced three-phase currents to the induction motor, as shown in Figure 5, confirming correct operation of the modulation strategy and current delivery prior to experimental implementation.

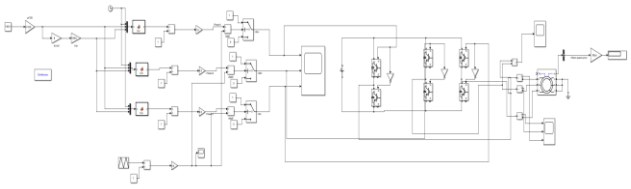

Figure 3. Simulink model in Simulink.

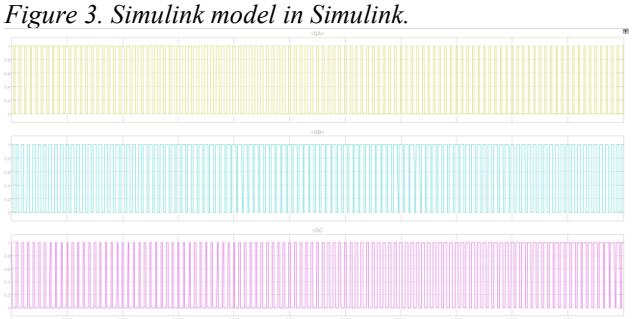

Figure 4. The three-phase SPWM signals generated by the Simulink model.

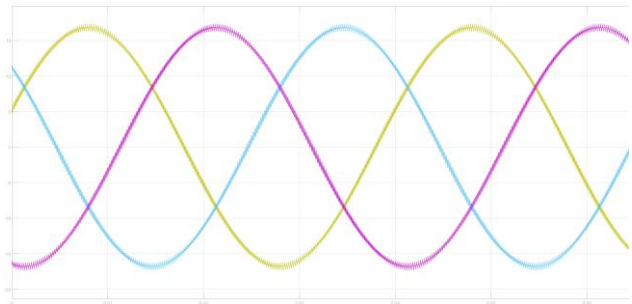

Figure 5. The three-phase current in the induction motor from the Simulink simulation.

Subsequently, the Verilog HDL logic was verified using Questa Simulation. Figure 6 illustrates the sawtooth carrier waveform and the resulting dead time between complementary switches. The measured dead time in simulation was approximately 2.06 µS, closely matching the designed parameter of 2 µS

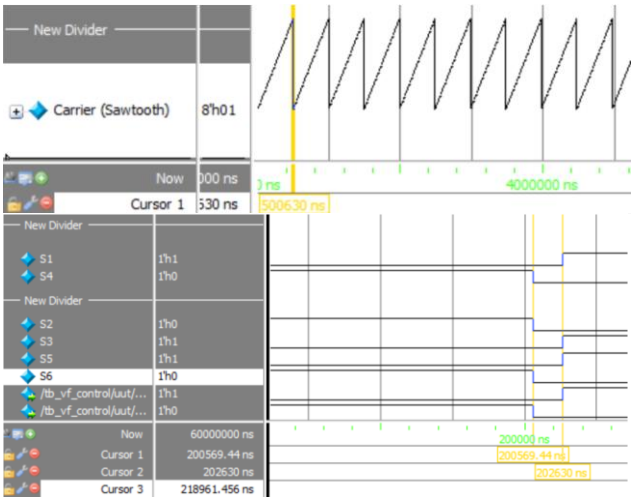

Figure 6. Simulation results: (a) Carrier waveform and (b) Dead time insertion.

Figure 7 shows the three-phase analog sine waves generated by the LUT at a voltage scaling factor of k = 100% The frequency corresponds to the rated 50 Hz. The logic successfully generates the necessary phase shifts of 120 degrees.

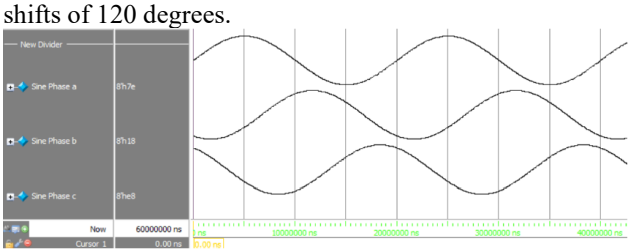

Figure 7. Three-phase analog sine waves at k = 100% (50 Hz).

Figure 8 displays the three-phase SPWM outputs for the switches at

. The pulses are distributed correctly across the period, and the modulation index is high, corresponding to full voltage.

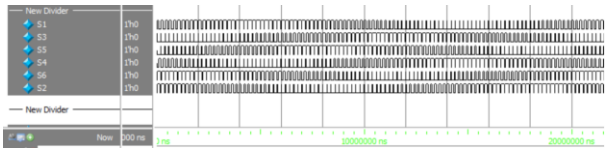

Figure 8. Three-phase SPWM outputs for the inverter switches at k = 100%.

II. Experimental Results

The experimental setup comprised the DE0-Nano FPGA, a three-phase inverter, an induction motor, and current transformers (CTs) for monitoring. The motor was commanded to operate at 500, 1000, and 2000 RPM via the UART interface.

The oscilloscope traces verified the high-side and low-side SPWM signals for Phase A. Figure 9 shows the Three-Phase SPWM signals for S1, S3, and S5 at 3000 rpm. The signals were correctly inverted with a visible dead time, confirming the safety of the switching logic, as detailed in Figure 10, which shows the dead time measured on the oscilloscope.

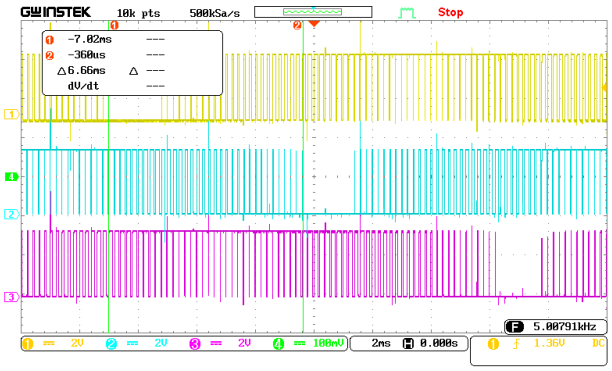

Figure 9. Three-Phase SPWM for S1, S3, and S5 at 3000 rpm.

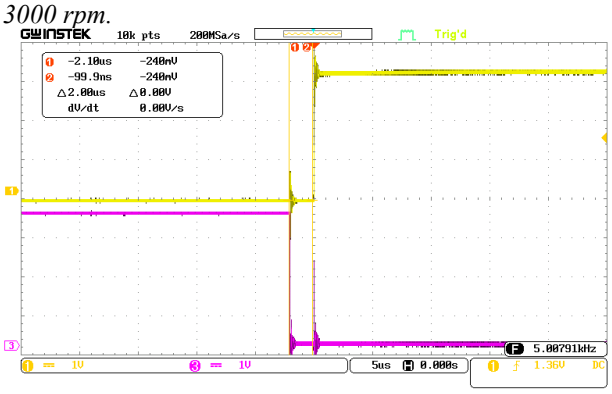

Figure 10. Dead time shown in the oscilloscope.

The three-phase motor currents were monitored at different speeds. Figure 11 shows the three-phase currents referred to the secondary side of the CT at a speed command of 500 RPM. The fundamental frequency of the current was measured to be 8.33 Hz, corresponding to a synchronous speed of 500 RPM according to (2).

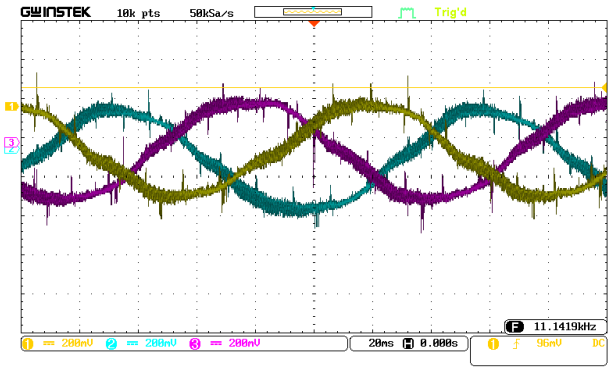

Figure 11. Three-phase currents referred to the secondary side of the CT at 500 rpm.

Similarly, tests at 1000 RPM and 2000 RPM yielded fundamental frequencies of 16.67 Hz and 33.33 Hz, respectively. The current waveforms for these speeds are presented in Figure 12 and Figure 13. The motor operated stably across all tested speeds, demonstrating the efficacy of the ramping algorithm and the V/f control logic.

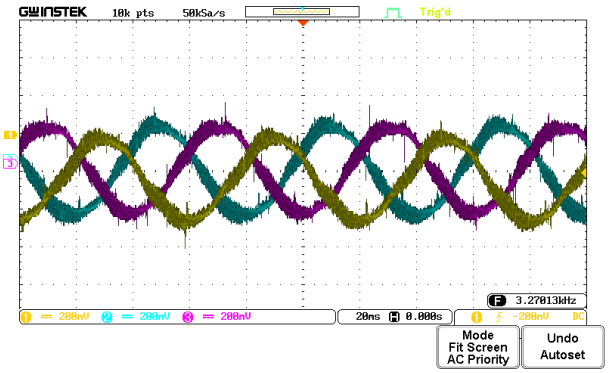

Figure 12. Three-phase currents referred to the secondary side of the CT at 1000 rpm.

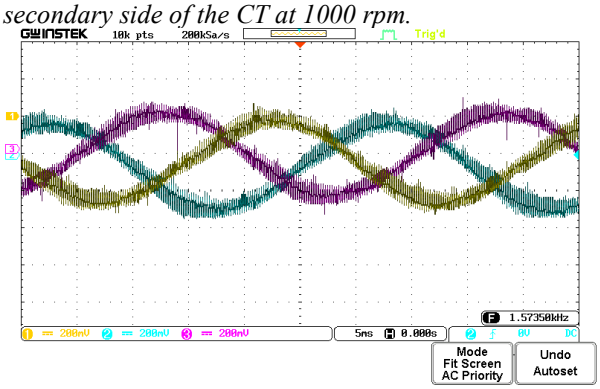

Figure 13. The three-phase currents referred to the secondary side of the CT at 2000 rpm.

CONCLUSTION

This project successfully developed a low-cost, high-quality induction motor control system using the V/f method implemented in Verilog HDL on the DE0-Nano FPGA. Unlike approaches dependent on specific Simulink toolboxes or expensive hardware, this design uses standard Verilog, ensuring portability and accessibility across various FPGA platforms. The inclusion of UART communication allowed for real-time speed adjustment, and the implementation of dead-time insertion ensured inverter safety.

Simulation and experimental results confirmed the system's ability to maintain the V/f ratio and drive the motor stably at commanded speeds. The project demonstrates that compact, low-cost FPGAs are a viable and economical alternative to DSP-based solutions for industrial motor control applications.

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